ABSTRACT OF THE DISCLOSURE

A stacked gate vertical flash memory and a fabrication method thereof. The stacked gate vertical flash memory comprises a semiconductor substrate with a trench, a source conducting layer formed on the bottom of the trench, an insulating layer formed on the source conducting layer, a gate dielectric layer formed on a sidewall of the trench, a conducting spacer covering the gate dielectric layer as a floating gate, an inter-gate dielectric layer covering the conducting spacer, and a control gate conducting layer filled in the trench.